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(54) **UNIT PIXEL AND ORGANIC LIGHT
EMITTING DISPLAY DEVICE INCLUDING
THE SAME**

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(57) **ABSTRACT**

A unit pixel includes a circuit structure, first and second wiring patterns, an interlayer insulating layer, a planarization layer, and a light emission structure. The first wiring pattern disposed on the circuit structure has a first bump structure. The interlayer insulating layer covers the circuit structure and the first wiring pattern. The second wiring pattern disposed on the interlayer insulating layer overlaps the first wiring pattern and has a second bump structure. The planarization layer covers the interlayer insulating layer and the second wiring pattern and includes a via-hole exposing at least a portion of the second wiring pattern. The light emission structure contacts the second wiring pattern through the via-hole. The first and second wiring patterns and the interlayer insulating layer form a capacitor, the light emission structure includes an OLED, and the capacitor is directly connected to an anode of the OLED.

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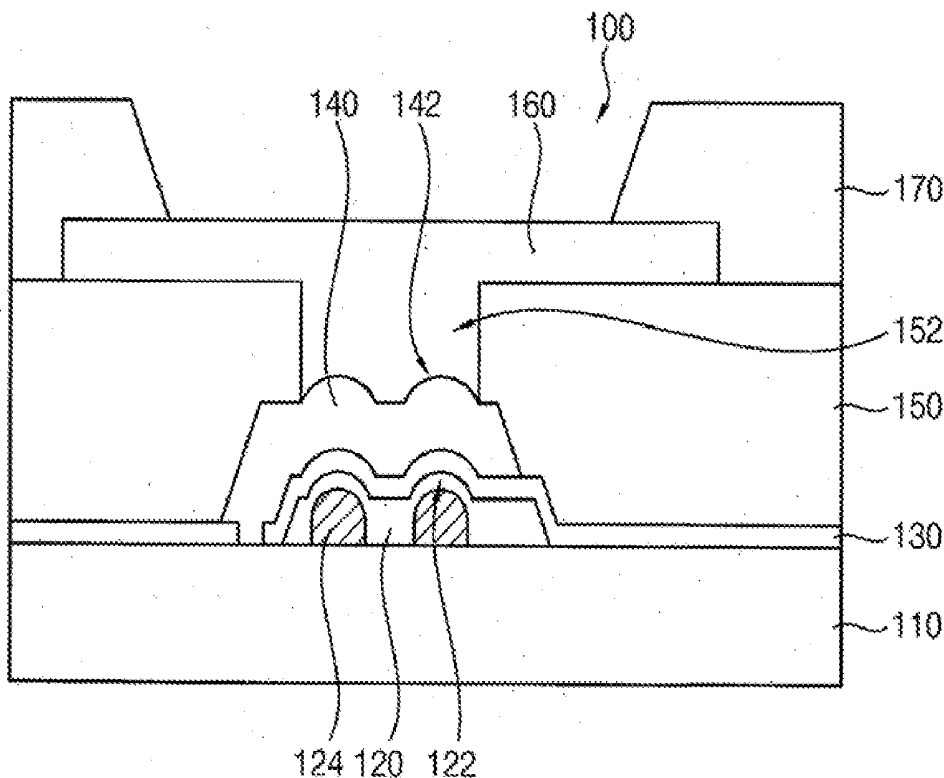


FIG. 1

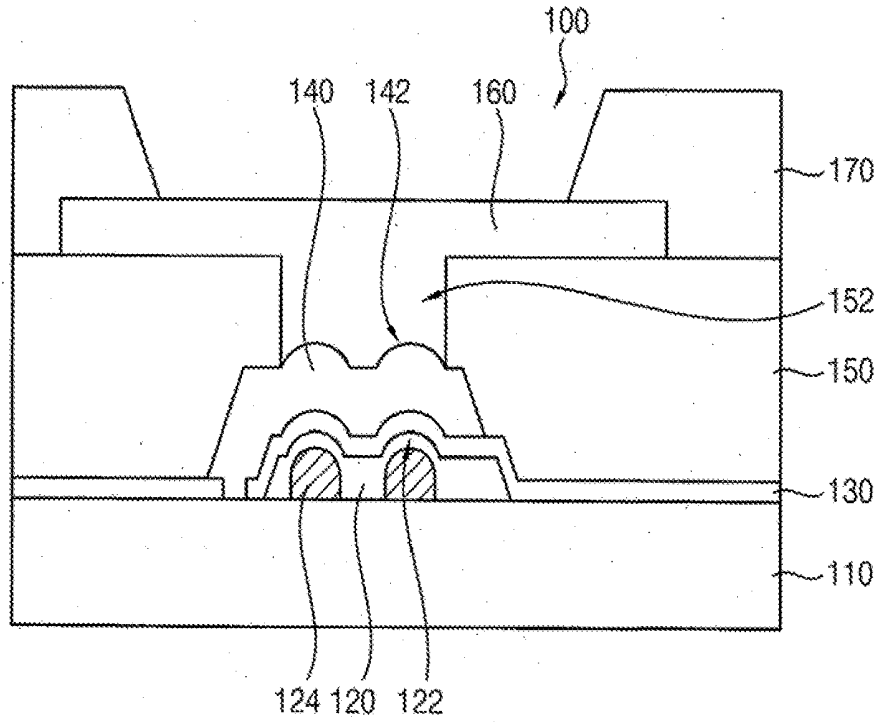


FIG. 2

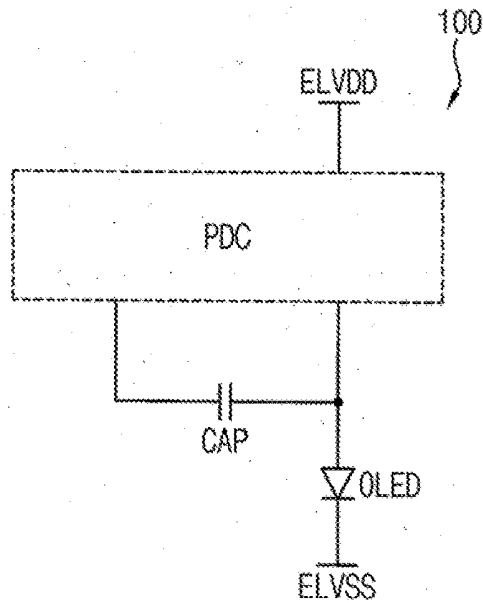


FIG. 3

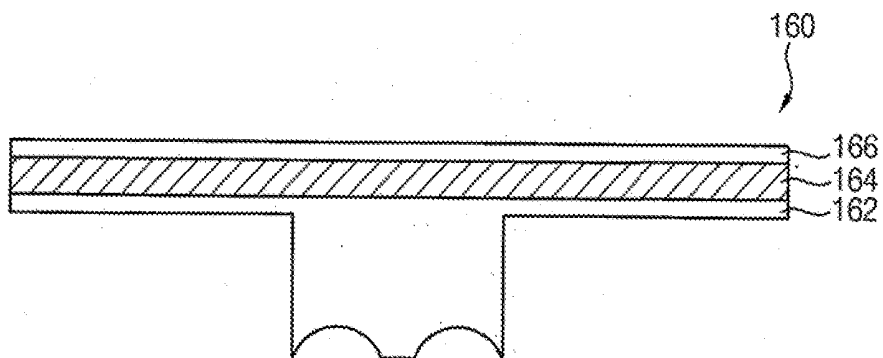


FIG. 4

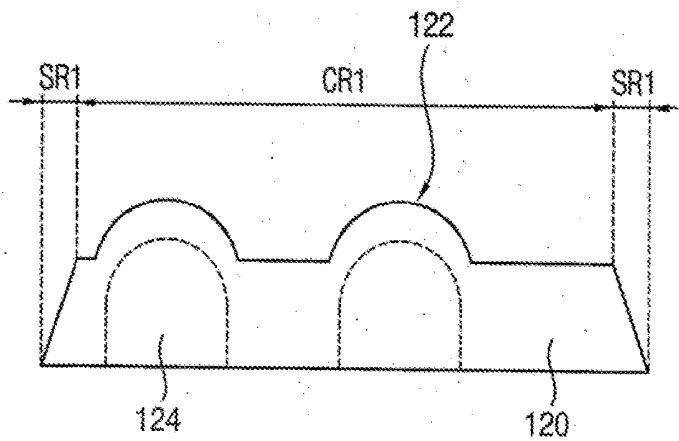


FIG. 5

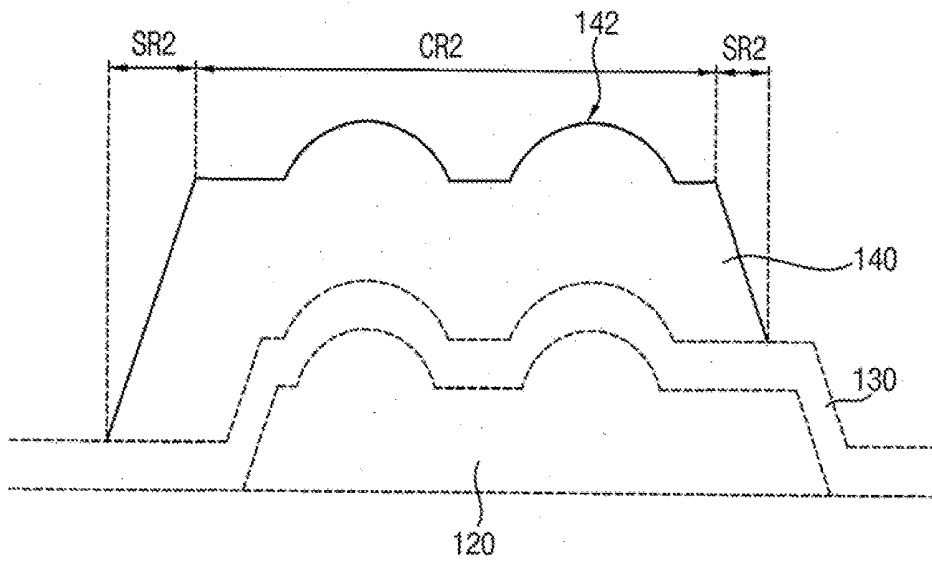


FIG. 6

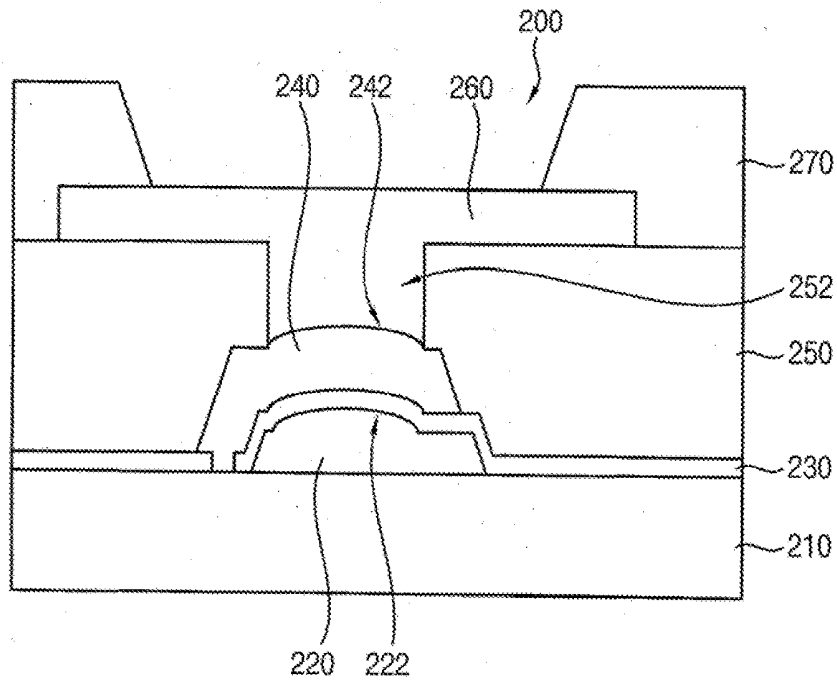


FIG. 7

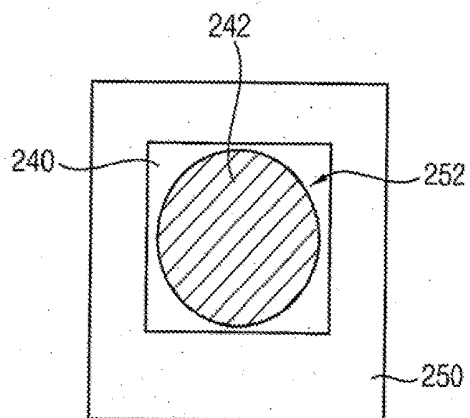


FIG. 8

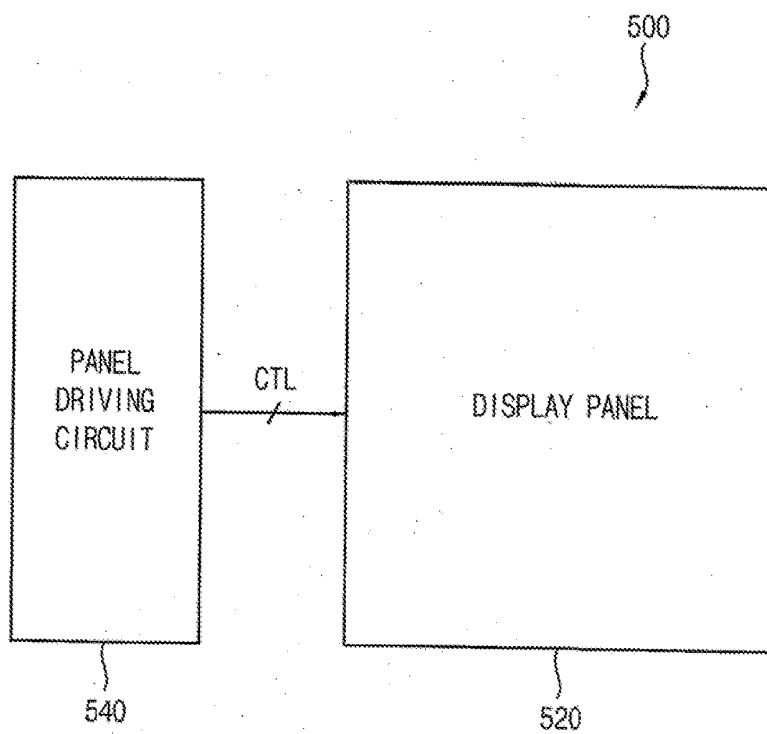


FIG. 9

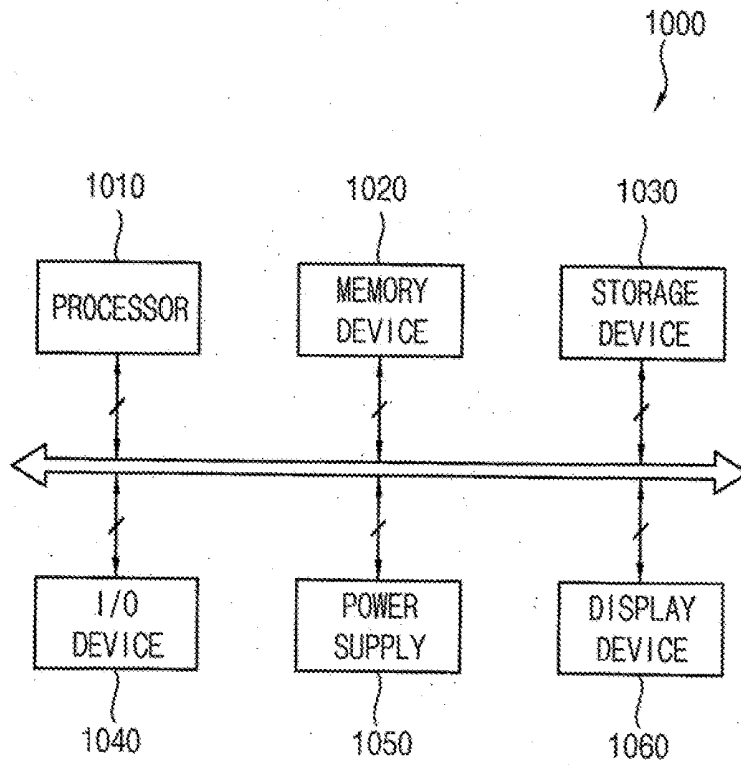
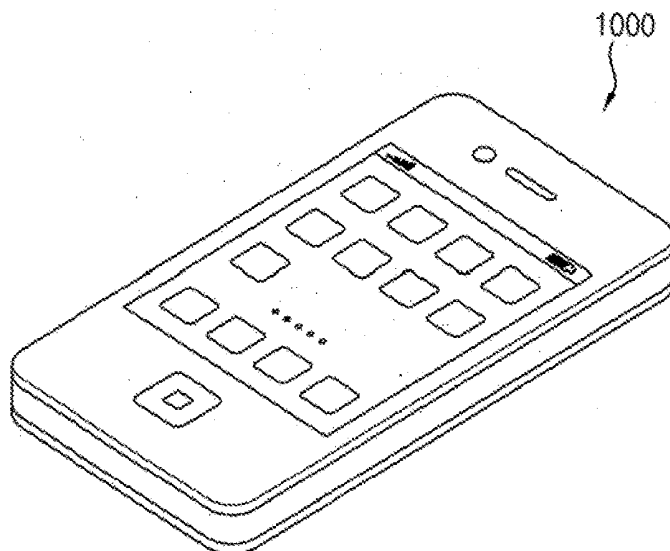


FIG. 10



**UNIT PIXEL AND ORGANIC LIGHT
EMITTING DISPLAY DEVICE INCLUDING
THE SAME**

CROSS-REFERENCE TO RELATED
APPLICATIONS

[0001] This application claims priority under 35 USC § 119 to Korean Patent Application No. 10-2017-0075135, filed on Jun. 14, 2017 in the Korean Intellectual Property Office (KIPO), the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

1. Technical Field

[0002] Exemplary embodiments of the present disclosure relate generally to a display device. More particularly, embodiments of the present inventive concept relate to a unit pixel that emits light using an organic light emitting diode and an organic light emitting display device including the unit pixel.

2. Description of the Related Art

[0003] Generally, an organic light emitting display (OLED) device includes a plurality of unit pixels, and each unit pixel has at least one transistor, at least one capacitor, and an organic light emitting diode. The organic light emitting display device controls light emission of each unit pixel by adjusting a current flowing through the organic light emitting diode in each unit pixel. As the capacitance of the capacitor included in each unit pixel increases, higher light emission luminance can be achieved because a loss of a data signal applied to each unit pixel via a data-line is reduced. The capacitance of the capacitor included in each unit pixel may be increased by increasing a size of both electrodes of the capacitor, decreasing a thickness of a dielectric layer disposed between the electrodes of the capacitor, and/or increasing a dielectric constant of the dielectric layer of the capacitor. However, increasing the size of the electrodes of the capacitor may be limited according to design constraints of the unit pixel, decreasing the thickness of the dielectric layer (e.g., an interlayer insulating layer) disposed between the electrodes (e.g., wiring patterns) of the capacitor may result in an electric short circuit, and increasing the dielectric constant of the dielectric layer of the capacitor may require a new material for the dielectric layer. Thus, it is desirable to increase the capacitance of the capacitor included in each unit pixel without changing the size of the electrodes of the capacitor, the thickness of the dielectric layer of the capacitor, and the dielectric constant or the dielectric material of the dielectric layer of the capacitor.

SUMMARY

[0004] Some exemplary embodiments of the present disclosure provide a unit pixel of an organic light emitting display device including a capacitor having increased capacitance due to an increased surface area of both electrodes of the capacitor without changing a size of the electrodes.

[0005] Some exemplary embodiments provide an organic light emitting display device including the unit pixel.

[0006] According to exemplary embodiments, a unit pixel may include a circuit structure, a first wiring pattern dis-

posed on the circuit structure, where the first wiring pattern has a first bump structure, an interlayer insulating layer covering the circuit structure and the first wiring pattern, a second wiring pattern disposed on the interlayer insulating layer, where the second wiring pattern overlaps the first wiring pattern and has a second bump structure corresponding to the first bump structure, a planarization layer covering the interlayer insulating layer and the second wiring pattern and including a via-hole that exposes at least a portion of the second wiring pattern, and a light emission structure contacting the second wiring pattern through the via-hole. The first wiring pattern, the interlayer insulating layer, and the second wiring pattern may form a capacitor, the light emission structure may include an organic light emitting diode, and the capacitor may be directly connected to an anode of the organic light emitting diode.

[0007] In exemplary embodiments, the first bump structure may include at least one first protrusion that protrudes in an upward direction.

[0008] In exemplary embodiments, the first wiring pattern may include a central region and a stepped portion region, and the first protrusion is disposed only in the central region.

[0009] In exemplary embodiments, the first bump structure may include a protrusion structure that is formed on the circuit structure corresponding to the first protrusion and the first wiring pattern that covers the protrusion structure.

[0010] In exemplary embodiments, the protrusion structure may include an organic material.

[0011] In exemplary embodiments, the organic material may include at least one of polyimide and siloxane.

[0012] In exemplary embodiments, the first bump structure may include the first wiring pattern that is formed on the circuit structure and the first protrusion that is formed by etching the first wiring pattern.

[0013] In exemplary embodiments, a cross-section of the first protrusion may be a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

[0014] In exemplary embodiments, the second bump structure may include at least one second protrusion that protrudes in an upward direction.

[0015] In exemplary embodiments, the second wiring pattern may include a central region and a stepped portion region, and the second protrusion may be disposed only in the central region.

[0016] In exemplary embodiments, the via-hole may entirely expose the second protrusion.

[0017] In exemplary embodiments, the via-hole may expose a portion of the second protrusion.

[0018] In exemplary embodiments, the second bump structure may include the interlayer insulating layer that is formed on the first wiring pattern and the second wiring pattern that is formed on the interlayer insulating layer.

[0019] In exemplary embodiments, a cross-section of the second protrusion may be a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

[0020] In exemplary embodiments, the first wiring pattern may be a data-line pattern or may be connected to the data-line pattern.

[0021] In exemplary embodiments, the second wiring pattern may be connected to one electrode of a driving transistor that is included in the circuit structure.

[0022] In exemplary embodiments, the first wiring pattern and the second wiring pattern may include a metal.

[0023] In exemplary embodiments, the light emission structure may include a first electrode pattern contacting the second wiring pattern through the via-hole, where the first electrode pattern corresponds to the anode of the organic light emitting diode, an organic layer disposed on the first electrode pattern, and a second electrode pattern disposed on the organic layer, where the second electrode pattern corresponds to a cathode of the organic light emitting diode.

[0024] According to exemplary embodiments, an organic light emitting display device may include a display panel including a plurality of unit pixels and a panel driving circuit configured to drive the display panel. Each of the unit pixels may include a circuit structure, a first wiring pattern disposed on the circuit structure, where the first wiring pattern has a first bump structure, an interlayer insulating layer covering the circuit structure and the first wiring pattern, a second wiring pattern disposed on the interlayer insulating layer, where the second wiring pattern overlaps the first wiring pattern and has a second bump structure corresponding to the first bump structure, a planarization layer covering the interlayer insulating layer and the second wiring pattern and including a via-hole that exposes at least a portion of the second wiring pattern, and a light emission structure contacting the second wiring pattern through the via-hole. The first wiring pattern, the interlayer insulating layer, and the second wiring pattern may form a capacitor, the light emission structure may include an organic light emitting diode, and the capacitor may be directly connected to an anode of the organic light emitting diode.

[0025] In exemplary embodiments, the first bump structure may include at least one first protrusion that protrudes in an upward direction, the second bump structure may include at least one second protrusion that protrudes in the upward direction, and cross-sections of the first protrusion and the second protrusion may be a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

[0026] Therefore, a unit pixel according to exemplary embodiments may have a capacitor that is directly connected to an anode of an organic light emitting diode and formed by a first wiring pattern having a first bump structure, an interlayer insulating layer covering the first wiring pattern, and a second wiring pattern overlapping the first wiring pattern and having a second bump structure corresponding to the first bump structure. Thus, the capacitance of the capacitor included in the unit pixel may be effectively increased by increasing a surface area of both electrodes (i.e., the first wiring pattern and the second wiring pattern) of the capacitor using the first bump structure and the second bump structure without changing a size of the electrodes of the capacitor.

[0027] In addition, an organic light emitting display device including the unit pixel according to exemplary embodiments may implement (or achieve) sufficient light emission luminance by reducing (or minimizing) a loss of a data signal applied to the unit pixel via a data-line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Illustrative, non-limiting exemplary embodiments will be more clearly understood from the following detailed description in conjunction with the accompanying drawings.

[0029] FIG. 1 is a diagram illustrating a unit pixel according to one exemplary embodiment.

[0030] FIG. 2 is a circuit diagram illustrating an example of the unit pixel of FIG. 1.

[0031] FIG. 3 is a diagram illustrating a light emission structure of the unit pixel of FIG. 1.

[0032] FIG. 4 is a diagram illustrating a first wiring pattern in the unit pixel of FIG. 1.

[0033] FIG. 5 is a diagram illustrating a second wiring pattern in the unit pixel of FIG. 1.

[0034] FIG. 6 is a diagram illustrating a unit pixel according to another exemplary embodiment.

[0035] FIG. 7 is a diagram illustrating a second protrusion of a second wiring pattern shown through a via-hole of a planarization layer included in the unit pixel of FIG. 6.

[0036] FIG. 8 is a diagram illustrating an organic light emitting display device according to one exemplary embodiment.

[0037] FIG. 9 is a block diagram illustrating an electronic device according to one exemplary embodiment.

[0038] FIG. 10 is a diagram illustrating an example in which the electronic device of FIG. 9 is implemented as a smart phone.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0039] Hereinafter, embodiments of the present inventive concept will be explained in detail with reference to the accompanying drawings.

[0040] FIG. 1 is a diagram illustrating a unit pixel according to one exemplary embodiment. FIG. 2 is a circuit diagram illustrating an example of the unit pixel of FIG. 1. FIG. 3 is a diagram illustrating a light emission structure of the unit pixel of FIG. 1.

[0041] Referring to FIGS. 1 to 3, the unit pixel 100 may be included in an organic light emitting display device. The unit pixel 100 may include a circuit structure 110, a first wiring pattern 120, an interlayer insulating layer 130, a second wiring pattern 140, a planarization layer 150, and a light emission structure 160. The unit pixel 100 may be defined by a pixel defining layer 170. The unit pixel 100 has a capacitor CAP that is directly connected to an anode of an organic light emitting diode OLED. For convenience of description, in FIGS. 1 and 2, the unit pixel 100 is illustrated focusing on the capacitor CAP and the organic light emitting diode OLED.

[0042] The circuit structure 110 may include components such as a transistor, a capacitor, etc. As illustrated in FIG. 2, a pixel driving circuit PDC may control light emission by adjusting a current flowing through the organic light emitting diode OLED between a high voltage ELVDD and a low voltage ELVSS. Thus, the circuit structure 110 may include components for performing the operation of the pixel driving circuit PDC. The first wiring pattern 120 may be disposed on the circuit structure 110. The first wiring pattern 120 may have a first bump structure. As illustrated in FIG. 1, the first bump structure may include at least one first protrusion 122 that protrudes in an upward direction. The first bump structure may include a protrusion structure 124 that is formed on the circuit structure 110 corresponding to the first protrusion 122 and the first wiring pattern 120 that covers the protrusion structure 124. Since the first wiring pattern 120 is formed after the protrusion structure 124 is formed on the circuit structure 110, a location corresponding to the protrusion structure 124 may protrude in the upward direction when the first wiring pattern 120 is formed, such that the first protrusion 122 may be formed. In an exemplary embodiment, the protrusion structure 124 may include an

organic material to prevent a defect such as an electric short circuit in a following process (e.g., a process for laminating metal patterns such as the first wiring pattern 120 and the second wiring pattern 140). For example, the protrusion structure 124 may include an organic material such as polyimide, siloxane, etc. However, the organic material for forming the protrusion structure 124 is not limited thereto. Although it is illustrated in FIG. 1 that a cross-section of the first protrusion 122 is a part of a circular shape, in some exemplary embodiments, the cross-section of the first protrusion 122 may be a part of an elliptical shape or a part of a polygonal shape.

[0043] The interlayer insulating layer 130 may cover the circuit structure 110 and the first wiring pattern 120. Since the first wiring pattern 120 includes the first protrusion 122 that protrudes in the upward direction, the interlayer insulating layer 130 that is formed on the first wiring pattern 120 may have a protrusion at a location corresponding to the first protrusion 122 in the upward direction. The second wiring pattern 140 may be disposed on the interlayer insulating layer 130. The second wiring pattern 140 may overlap the first wiring pattern 120. In addition, the second wiring pattern 140 may have a second bump structure corresponding to the first bump structure. As illustrated in FIG. 1, the second bump structure may include at least one second protrusion 142 that protrudes in the upward direction. The second bump structure may include the interlayer insulating layer 130 that is formed on the first wiring pattern 120 and the second wiring pattern 140 that is formed on the interlayer insulating layer 130. Since the interlayer insulating layer 130 that is formed on the first wiring pattern 120 has a protrusion at a location corresponding to the first protrusion 122 in the upward direction and since the second wiring pattern 140 that overlaps the first wiring pattern 120 is formed on the interlayer insulating layer 130, a location corresponding to the first protrusion 122 may protrude in the upward direction when the second wiring pattern 140 is formed, such that the second protrusion 142 may be formed. Although it is illustrated in FIG. 1 that a cross-section of the second protrusion 142 is a part of a circular shape, in some exemplary embodiments, the cross-section of the second protrusion 142 may be a part of an elliptical shape or a part of a polygonal shape. A shape of the second protrusion 142 included in the second wiring pattern 140 may be determined by a shape of the first protrusion 122 included in the first wiring pattern 120, and the shape of the first protrusion 122 included in the first wiring pattern 120 may be determined by a shape of the protrusion structure 124.

[0044] The planarization layer 150 may cover the interlayer insulating layer 130 and the second wiring pattern 140 and may include a via-hole 152 that exposes at least a portion of the second wiring pattern 140. In an exemplary embodiment, as illustrated FIG. 1, the via-hole 152 of the planarization layer 150 may entirely expose the second protrusion 142 included in the second wiring pattern 140. In this case, the via-hole 152 may be filled with a metal (i.e., a first electrode pattern 162 of the light emission structure 160), such that the second wiring pattern 140 may contact the light emission structure 160. Thus, a stepped portion due to the second protrusion 142 of the second wiring pattern 140 may be covered by the metal in the via-hole 152 to prevent a structural distortion that may be caused by the second protrusion 142 of the second wiring pattern 140. In some exemplary embodiments, the via-hole 152 of the

planarization layer 150 may expose only a portion of the second protrusion 142 of the second wiring pattern 140. The light emission structure 160 may contact the second wiring pattern 140 through the via-hole 152 of the planarization layer 150. In an exemplary embodiment, as illustrated in FIG. 3, the light emission structure 160 may include a first electrode pattern 162 (herein also referred to as a pixel electrode or an anode), an organic layer 164, and a second electrode pattern 166 (herein also referred to as an opposing electrode or a cathode). The first electrode pattern 162 may contact the second wiring pattern 140 through the via-hole 152 of the planarization layer 150. For example, the first electrode pattern 162 may be an anode of the organic light emitting diode OLED. The organic layer 164 may be disposed on the first electrode pattern 162. Specifically, the organic layer 164 may include a hole injection layer, a hole transport layer, a light emission layer, an electron transport layer, and an electron injection layer. The second electrode pattern 166 may be disposed on the organic layer 164. For example, the second electrode pattern 166 may be a cathode of the organic light emitting diode OLED. In some exemplary embodiments, the light emission structure 160 (i.e., the organic light emitting diode OLED) may have an internal resonance structure to achieve relatively high light emission efficiency. In this case, the first electrode pattern 162 or the second electrode pattern 164 of the light emission structure 160 may be a reflective electrode pattern.

[0045] As described above, in the unit pixel 100, the first wiring pattern 120, the interlayer insulating layer 130, and the second wiring pattern 140 may form the capacitor CAP illustrated in FIG. 2, the light emission structure 160 may include the organic light emitting diode OLED illustrated in FIG. 2, and the capacitor CAP may be directly connected to the anode of the organic light emitting diode OLED. In other words, the first wiring pattern 120 may correspond to one electrode of the capacitor CAP, the second wiring pattern 140 may correspond to another electrode of the capacitor CAP, and the interlayer insulating layer 130 may correspond to the dielectric layer of the capacitor CAP. Each of the first wiring pattern 120 and the second wiring pattern 140 may include a metal. Since the first wiring pattern 120 has the first bump structure, a surface area of the first wiring pattern 120 may be increased. In addition, since the second wiring pattern 140 has the second bump structure, a surface area of the second wiring pattern 140 may be increased. The capacitor CAP may include the first wiring pattern 120 including the first protrusion 122 that protrudes in the upward direction and the second wiring pattern 140 including the second protrusion 142 that protrudes in the upward direction. As a result, the capacitor CAP may have increased capacitance without changing a size of both electrodes (i.e., the first and second wiring patterns 120 and 140) of the capacitor CAP. In some exemplary embodiments, according to a structure of the unit pixel 100, the first wiring pattern 120 may be a data-line pattern through which a data signal is transferred or may be connected to the data-line pattern. In addition, the second wiring pattern 140 may be connected to an electrode of a driving transistor included in the circuit structure 110. The unit pixel 100 may have the capacitor CAP that is directly connected to the anode of the organic light emitting diode OLED and formed by the first wiring pattern 120 having the first bump structure, the interlayer insulating layer 130 that covers the first wiring pattern 120, and the second wiring pattern 140 that overlaps the first wiring

pattern 120 and having the second bump structure corresponding to the first bump structure. Thus, the unit pixel 100 may effectively increase the capacitance of the capacitor CAP by increasing the surface area of both electrodes (i.e., the first wiring pattern 120 and the second wiring pattern 140) of the capacitor CAP using the first bump structure and the second bump structure without changing a size of the electrodes of the capacitor.

[0046] FIG. 4 is a diagram illustrating a first wiring pattern in the unit pixel of FIG. 1. FIG. 5 is a diagram illustrating a second wiring pattern in the unit pixel of FIG. 1.

[0047] Referring to FIGS. 4 and 5, the interlayer insulating layer 130 may be formed on the first wiring pattern 120 after the first wiring pattern 120 is formed, and the second wiring pattern 140 may be formed on the interlayer insulating layer 130 after the interlayer insulating layer 130 is formed.

[0048] As illustrated in FIG. 4, the first wiring pattern 120 may have a first bump structure, and the first bump structure may include at least one first protrusion 122 that protrudes in an upward direction. Since the first wiring pattern 120 is formed after a protrusion structure 124 is formed on a circuit structure 110, a location corresponding to the protrusion structure 124 may protrude in the upward direction when the first wiring pattern 120 is formed, such that the first protrusion 122 may be formed. Thus, a shape of the first protrusion 122 included in the first wiring pattern 120 may be determined by a shape of the protrusion structure 124. The first wiring pattern 120 may include a central region CR1 and a stepped portion region SR1, and the first protrusion 122 may be disposed only in the central region CR1. This is because a defect caused by the first protrusion 122 may occur in a following process if the first protrusion 122 is formed in the stepped portion region SR1. For example, in the first wiring pattern 120, the first protrusion 122 may be formed in the central region CR1 as being spaced apart from a boundary between the central region CR1 and the stepped portion region SR1 by at least more than 1 μm . As illustrated in FIG. 5, the interlayer insulating layer 130 may be formed on the first wiring pattern 120. Since the first wiring pattern 120 includes the first protrusion 122 that protrudes in the upward direction, the interlayer insulating layer 130 formed on the first wiring pattern 120 may have a protrusion at a location corresponding to the first protrusion 122 in the upward direction. The second wiring pattern 140 may be formed on the interlayer insulating layer 130. The second wiring pattern 140 may have a second bump structure, and the second bump structure may include at least one second protrusion 142 that protrudes in the upward direction. Since the interlayer insulating layer 130 formed on the first wiring pattern 120 has the protrusion at a location corresponding to the first protrusion 122 in the upward direction and since the second wiring pattern 140 that overlaps the first wiring pattern 120 is formed on the interlayer insulating layer 130, a location corresponding to the first protrusion 122 may protrude in the upward direction when the second wiring pattern 140 is formed, such that the second protrusion 142 may be formed. Thus, a shape of the second protrusion 142 included in the second wiring pattern 140 may be determined by a shape of the first protrusion 122 included in the first wiring pattern 120. The second wiring pattern 140 may include a central region CR2 and a stepped portion region SR2, and the second protrusion 142 may be disposed only in the central region CR2. This is because a defect caused by the second protrusion 142 may occur in a following process if the

second protrusion 142 is formed in the stepped portion region SR2. For example, in the second wiring pattern 140, the second protrusion 142 may be formed in the central region CR2 as being spaced apart from a boundary between the central region CR2 and the stepped portion region SR2 by at least more than 1 μm . Although it is illustrated in FIGS. 4 and 5 that cross-sections of the first protrusion 122 and the second protrusion 142 are a part of a circular shape, in some exemplary embodiments, the cross-sections of the first protrusion 122 and the second protrusion 142 may be a part of an elliptical shape or a part of a polygonal shape.

[0049] FIG. 6 is a diagram illustrating a unit pixel according to another exemplary embodiment. FIG. 7 is a diagram illustrating a second protrusion of a second wiring pattern shown through a via-hole of a planarization layer included in the unit pixel of FIG. 6.

[0050] Referring to FIG. 6 and 7, the unit pixel 200 included in an organic light emitting display device may include a circuit structure 210, a first wiring pattern 220, an interlayer insulating layer 230, a second wiring pattern 240, a planarization layer 250, and a light emission structure 260. The unit pixel 200 may be defined by a pixel defining layer 270. The unit pixel 200 has a capacitor that is directly connected to an anode of an organic light emitting diode. For convenience of description, in FIG. 6, the unit pixel 200 is illustrated focusing on the capacitor and the organic light emitting diode.

[0051] The circuit structure 210 may include components such as a transistor, a capacitor, etc. The first wiring pattern 220 may be disposed on the circuit structure 210. The first wiring pattern 220 may have a first bump structure. As illustrated in FIG. 6, the first bump structure may include at least one first protrusion 222 that protrudes in an upward direction. The first bump structure may include the first wiring pattern 220 that is formed on the circuit structure 210 and the first protrusion 222 that is formed by etching the first wiring pattern 220. The interlayer insulating layer 230 may cover the circuit structure 210 and the first wiring pattern 220. Since the first wiring pattern 220 includes the first protrusion 222 that protrudes in the upward direction, the interlayer insulating layer 230 formed on the first wiring pattern 220 may have a protrusion at a location corresponding to the first protrusion 222 in the upward direction. The second wiring pattern 240 may be disposed on the interlayer insulating layer 230. The second wiring pattern 240 may overlap the first wiring pattern 220. In addition, the second wiring pattern 240 may have a second bump structure corresponding to the first bump structure. As illustrated in FIG. 6, the second bump structure may include at least one second protrusion 242 that protrudes in the upward direction. The second bump structure may include the interlayer insulating layer 230 that is formed on the first wiring pattern 220 and the second wiring pattern 240 that is formed on the interlayer insulating layer 230. Since the interlayer insulating layer 230 that is formed on the first wiring pattern 220 has a protrusion at a location corresponding to the first protrusion 222 in the upward direction and since the second wiring pattern 240 that overlaps the first wiring pattern 220 is formed on the interlayer insulating layer 230, a location corresponding to the first protrusion 222 may protrude in the upward direction when the second wiring pattern 240 is formed, such that the second protrusion 242 may be formed. A shape of the second protrusion 242 included in the second

wiring pattern 240 may be determined by a shape of the first protrusion 222 included in the first wiring pattern 220.

[0052] The planarization layer 250 may cover the interlayer insulating layer 230 and the second wiring pattern 240 and may include a via-hole 252 that exposes at least a portion of the second wiring pattern 240. In an exemplary embodiment, as illustrated in FIGS. 6 and 7, the via-hole 252 of the planarization layer 250 may entirely expose the second protrusion 242 included in the second wiring pattern 240. In this case, the via-hole 252 may be filled with a metal (i.e., a first electrode pattern 262 of the light emission structure 260), such that the second wiring pattern 240 may contact the light emission structure 260. A stepped portion caused by the second protrusion 242 of the second wiring pattern 240 may be covered by the metal in the via-hole 252 to prevent a structural distortion that may be caused by the second protrusion 242 of the second wiring pattern 240. In some exemplary embodiments, the via-hole 252 of the planarization layer 250 may expose only a portion of the second protrusion 242 of the second wiring pattern 240. The light emission structure 260 may contact the second wiring pattern 240 through the via-hole 252 of the planarization layer 250. In an exemplary embodiment, the light emission structure 260 may include as first electrode pattern, an organic layer, and a second electrode pattern. The first electrode pattern may contact the second wiring pattern 240 through the via-hole 252 of the planarization layer 250. For example, the first electrode pattern may be an anode of the organic light emitting diode. The organic layer may be disposed on the first electrode pattern. Specifically, the organic layer may include a hole injection layer, a hole transport layer, a light emission layer, an electron transport layer, and an electron injection layer. The second electrode pattern may be disposed on the organic layer. For example, the second electrode pattern may be a cathode of the organic light emitting diode. In some exemplary embodiments, the light emission structure 260 (i.e., the organic light emitting diode) may have an internal resonance structure to achieve relatively high light emission efficiency. In this case, the first electrode pattern or the second electrode pattern of the light emission structure 260 may be a reflective electrode pattern.

[0053] As described above, in the unit pixel 200, the first wiring pattern 220, the interlayer insulating layer 230, and the second wiring pattern 240 may form the capacitor, the light emission structure 260 may include the organic light emitting diode, and the capacitor may be directly connected to the anode of the organic light emitting diode. In other words, the first wiring pattern 220 may correspond to one electrode of the capacitor, the second wiring pattern 240 may correspond to another electrode of the capacitor, and the interlayer insulating layer 230 may correspond to the dielectric layer of the capacitor. Each of the first wiring pattern 220 and the second wiring pattern 240 may include a metal. Since the first wiring pattern 220 has the first bump structure, a surface area of the first wiring pattern 220 may be increased. In addition, since the second wiring pattern 240 has the second bump structure, a surface area of the second wiring pattern 240 may be increased. The capacitor may include the first wiring pattern 220 including the first protrusion 222 that protrudes in the upward direction and the second wiring pattern 240 including the second protrusion 242 that protrudes in the upward direction. As a result, the capacitor may have increased capacitance without changing a size of both electrodes (i.e., the first and second wiring

patterns 220 and 240) of the capacitor. The unit pixel 200 may have the capacitor that is directly connected to the anode of the organic light emitting diode and formed by the first wiring pattern 220 having the first bump structure, the interlayer insulating layer 230 that covers the first wiring pattern 220, and the second wiring pattern 240 that overlaps the first wiring pattern 220 and having the second bump structure corresponding to the first bump structure. Thus, the unit pixel 200 may effectively increase the capacitance of the capacitor by increasing the surface area of both electrodes (i.e., the first wiring pattern 220 and the second wiring pattern 240) of the capacitor using the first bump structure and the second bump structure without changing a size of the electrodes of the capacitor.

[0054] FIG. 8 is a diagram illustrating an organic light emitting display device according to one exemplary embodiment.

[0055] Referring to FIG. 8, the organic light emitting display device 500 may include a display panel 520 and a panel driving circuit 540 that drives the display panel 520.

[0056] The display panel 520 may include a plurality of unit pixels. Each of the unit pixels may have a capacitor that is directly connected to an anode of an organic light emitting diode. Specifically, each of the unit pixels may include a circuit structure, a first wiring pattern, an interlayer insulating layer, a second wiring pattern, a planarization layer, and a light emission structure. The first wiring pattern may be disposed on the circuit structure. The first wiring pattern may have a first bump structure. The interlayer insulating layer may cover the circuit structure and the first wiring pattern. The second wiring pattern may be disposed on the interlayer insulating layer. The second wiring pattern may overlap the first wiring pattern. The second wiring pattern may have a second bump structure corresponding to the first bump structure. The planarization layer may cover the interlayer insulating layer and the second wiring pattern. The planarization layer may include a via-hole that exposes at least a portion of the second wiring pattern. The light emission structure may contact the second wiring pattern through the via-hole. The first wiring pattern, the interlayer insulating layer, and the second wiring pattern may form the capacitor, and the light emission structure may include the organic light emitting diode. The first bump structure may include at least one first protrusion that protrudes in an upward direction. The second bump structure may include at least one second protrusion that protrudes in the upward direction. Cross-sections of the first protrusion and the second protrusion may be a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape. The display panel 520 may display an image based on lights output from the unit pixels. In an exemplary embodiment, the unit pixels included in the display panel 520 may include a red light emission pixel that outputs red light, a green light emission pixel that outputs green light, and a blue light emission pixel that outputs blue light. In another exemplary embodiment, the unit pixels included in the display panel 520 may include a red light emission pixel that outputs red light, a green light emission pixel that outputs green light, a blue light emission pixel that outputs blue light, and a white light emission pixel that outputs white light.

[0057] The panel driving circuit 540 may drive the display panel 520 by providing control signals to the display panel 520. Specifically, the panel driving circuit 540 may include a scan driver, a data driver, a timing controller, etc. The scan

driver may be connected to the display panel 520 via scan-lines. The scan driver may provide a scan signal to the unit pixels of the display panel 520 via the scan-lines. The data driver may be connected to the display panel 520 via data-lines. The data driver may convert image data provided by the timing controller into a data voltage (i.e., a data signal) and then may provide the data signal to the unit pixels of the display panel 520. In some exemplary embodiments, the timing controller may receive the image data from an external component, may perform a given processing (e.g., data compensation processing, etc), and may provide processed image data to the data driver. In some exemplary embodiments, the panel driving circuit 540 may further include an emission control driver. The emission control driver may be connected to the display panel 520 via emission control-lines. The emission control driver may provide an emission control signal to the unit pixels of the display panel 520 via the emission control-lines. Although it is described above that the organic light emitting display device 500 includes the display panel 520 and the panel driving circuit 540, and the panel driving circuit 540 includes the scan driver, the data driver, the timing controller, and the emission control driver, in some exemplary embodiments, the present disclosure is not limited thereto. For example, the organic emitting display device 500 may further include other components, for example, a deterioration compensating circuit that performs deterioration compensation for the unit pixels of the display panel 520. The organic light emitting display device 500 may include the unit pixels each including a capacitor having increased capacitance, where the capacitor includes the first wiring pattern having the first bump structure, the interlayer insulating layer covering the first wiring pattern, and the second wiring pattern overlapping the first wiring pattern and having the second bump structure corresponding to the first bump structure. Thus, the organic light emitting display device 500 may implement (or achieve) sufficient light emission luminance by reducing (or minimizing) a loss of the data signal applied to the unit pixel via the data-line. As a result, the organic light emitting display device 500 may provide a high-quality image to a viewer.

[0058] FIG. 9 is a block diagram illustrating an electronic device according to one exemplary embodiment. FIG. 10 is a diagram illustrating an example in which the electronic device of FIG. 9 is implemented as a smart phone.

[0059] Referring to FIGS. 9 and 10, the electronic device 1000 may include a processor 1010, a memory device 1020, a storage device 1030, an input/output (I/O) device 1040, a power supply 1050, and an organic light emitting display device 1060. The organic light emitting display device 1060 may be the organic light emitting display device 500 of FIG. 8. In addition, the electronic device 1000 may further include a plurality of ports for communicating with a video card, a sound card, a memory card, a universal serial bus (USB) device, other electronic devices, etc. In an exemplary embodiment, as illustrated in FIG. 10, the electronic device 1000 may be implemented as a smart phone. However, the electronic device 1000 is not limited thereto. For example, the electronic device 1000 may be implemented as a television, a cellular phone, a video phone, a smart pad, a smart watch, a tablet PC, a car navigation system, a computer monitor, a laptop, a head mounted display (HMD) device, etc.

[0060] The processor 1010 may perform various computing functions. The processor 1010 may be a micro processor, a central processing unit (CPU), an application processor (AP), etc. The processor 1010 may be coupled to other components via an address bus, a control bus, a data bus, etc. Further, the processor 1010 may be coupled to an extended bus such as a peripheral component interconnection (PCI) bus. The memory device 1020 may store data and instructions for operations of the electronic device 1000. For example, the memory device 1020 may include at least one non-volatile memory device such as an erasable programmable read-only memory (EPROM) device, an electrically erasable programmable read-only memory (EEPROM) device, a flash memory device, a phase change random access memory (PRAM) device, a resistance random access memory (RRAM) device, a nano floating gate memory (NPGM) device, a polymer random access memory (PoRAM) device, a magnetic random access memory (MRAM) device, a ferroelectric random access memory (FRAM) device, etc, and/or at least one volatile memory device such as a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a mobile DRAM device, etc. The storage device 1030 may be a solid-state drive (SSD) device, a hard disk drive (HDD) device, a CD-ROM device, etc. The I/O device 1040 may include an input device such as a keyboard, a keypad, a mouse device, a touchpad, a touch-screen, a remote controller, etc, and output device such as a printer, a speaker, etc. In some exemplary embodiments, the organic light emitting-display device 1060 may be included in the I/O device 1040. The power supply 1050 may provide power for operations of the electronic device 1000.

[0061] The organic light emitting display device 1060 may be coupled to other components via the buses or other communication links. As described above, the organic light emitting display device 1060 may include a display panel including a plurality of unit pixels and a panel driving circuit that drives the display panel. Each of the unit pixels may have a capacitor that is directly connected to an anode of an organic light emitting diode. Specifically, each of the unit pixels may include a circuit structure, a first wiring pattern, an interlayer insulating layer, a second wiring pattern, a planarization layer, and a light emission structure. The first wiring pattern may be disposed on the circuit structure. The first wiring pattern may have a first bump structure. The interlayer insulating layer may cover the circuit structure and the first wiring pattern. The second wiring pattern may be disposed on the interlayer insulating layer. The second wiring pattern may overlap the first wiring pattern and may have a second bump structure corresponding to the first bump structure. The planarization layer may cover the interlayer insulating layer and the second wiring pattern. The planarization layer may include a via-hole that expose at least a portion of the second wiring pattern. The light emission structure may contact the second wiring pattern through the via-hole. The first wiring pattern, the interlayer insulating layer, and the second wiring pattern may form the capacitor, and the light emission structure may include the organic light emitting diode. The first bump structure may include at least one first protrusion that protrudes in an upward direction. The second bump structure may include at least one second protrusion that protrudes in the upward direction. In exemplary embodiments, cross-sections of the first protrusion and the second protrusion may be a part of

a circular shape, a part of an elliptical shape, or a part of a polygonal shape. In each of the unit pixels, the capacitor may be formed by the first wiring pattern having the first bump structure, the interlayer insulating layer covering the first wiring pattern, and the second wiring pattern overlapping the first wiring pattern and having the second bump structure corresponding to the first bump structure. Thus, the capacitance of the capacitor included in each of the unit pixels may be effectively increased by increasing a surface area of both electrodes (i.e. the first wiring pattern and the second wiring pattern) of the capacitor using the first bump structure and the second bump structure without changing a size of the electrodes of the capacitor. As a result, the organic light emitting display device 1060 including the unit pixel may implement sufficient light emission luminance by reducing a loss of a data signal applied to the unit pixel via a data-line. Since these are described above, duplicated description related thereto will not be repeated.

[0062] The present inventive concept may be applied to an organic light emitting display device and an electronic device including the organic light emitting display device. For example, the present inventive concept may be applied to a cellular phone, a smart phone, a video phone, a smart pad, a smart watch, a tablet PC, a car navigation system, a television, a computer monitor, a laptop, a digital camera, an HMD device, etc.

[0063] The foregoing is illustrative of exemplary embodiments and is not to be construed as limiting thereof. Although a few exemplary embodiments have been described, those skilled in the art will readily appreciate that deviations and modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, such deviations and modifications are intended to be included within the scope of the present inventive concept of the present disclosure. Therefore, it is to be understood that the foregoing is illustrative of various exemplary embodiments and is not to be construed as limited to the specific exemplary embodiments disclosed, and that deviations and modifications to the disclosed exemplary embodiments, as well as other exemplary embodiments, are intended to be included within the scope of the present disclosure.

What is claimed is:

1. A unit pixel comprising:

a circuit structure;

a first wiring pattern disposed on the circuit structure, the first wiring pattern having a first bump structure;

an interlayer insulating layer covering the circuit structure and the first wiring pattern;

a second wiring pattern disposed on the interlayer insulating layer, the second wiring pattern overlapping the first wiring pattern and having a second bump structure corresponding to the first bump structure;

a planarization layer covering the interlayer insulating layer and the second wiring pattern and including a via-hole that exposes at least a portion of the second wiring pattern; and

a light emission structure contacting the second wiring pattern through the via-hole,

wherein the first wiring pattern, the interlayer insulating layer, and the second wiring pattern form a capacitor, the light emission structure includes an organic light

emitting diode, and the capacitor is directly connected to an anode of the organic light emitting diode.

2. The unit pixel of claim 1, wherein the first bump structure includes at least one first protrusion that protrudes in an upward direction.

3. The unit pixel of claim 2, wherein the first wiring pattern includes a central region and a stepped portion region, and the first protrusion is disposed only in the central region.

4. The unit pixel of claim 2, wherein the first bump structure includes a protrusion structure that is formed on the circuit structure corresponding to the first protrusion and the first wiring pattern that covers the protrusion structure.

5. The unit pixel of claim 4, wherein the protrusion structure includes an organic material.

6. The unit pixel of claim 5, wherein the organic material includes at least one of polyimide and siloxane.

7. The unit pixel of claim 2, wherein the first bump structure includes the first wiring pattern that is formed on the circuit structure and the first protrusion that is formed by etching the first wiring pattern.

8. The unit pixel of claim 2, wherein a cross-section of the first protrusion is a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

9. The unit pixel of claim 1, wherein the second bump structure includes at least one second protrusion that protrudes in an upward direction.

10. The unit pixel of claim 9, wherein the second wiring pattern includes a central region and a stepped portion region, and the second protrusion is disposed only in the central region.

11. The unit pixel of claim 9, wherein the via-hole entirely exposes the second protrusion.

12. The unit pixel of claim 9, wherein the via-hole exposes a portion of the second protrusion.

13. The unit pixel of claim 9, wherein the second bump structure includes the interlayer insulating layer that is formed on the first wiring pattern and the second wiring pattern that is formed on the interlayer insulating layer.

14. The unit pixel of claim 9, wherein a cross-section of the second protrusion is a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

15. The unit pixel of claim 1, wherein the first wiring pattern is a data-line pattern or is connected to the data-line pattern.

16. The unit pixel of claim 15, wherein the second wiring pattern is connected to one electrode of a driving transistor that is included in the circuit structure.

17. The unit pixel of claim 16, wherein the first wiring pattern and the second wiring pattern include a metal.

18. The unit pixel of claim 16, wherein the light emission structure includes:

a first electrode pattern contacting the second wiring pattern through the via-hole, the first electrode pattern corresponding to the anode of the organic light emitting diode;

an organic layer disposed on the first electrode pattern; and

a second electrode pattern disposed on the organic layer, the second electrode pattern corresponding to a cathode of the organic light emitting diode.

19. An organic light emitting display device comprising: a display panel including a plurality of unit pixels; and a panel driving circuit configured to drive the display panel,

wherein each of the unit pixels includes:

a circuit structure;

a first wiring pattern disposed on the circuit structure, the first wiring pattern having a first bump structure;

an interlayer insulating layer covering the circuit structure and the first wiring pattern,

a second wiring pattern disposed on the interlayer insulating layer, the second wiring pattern overlapping the first wiring pattern and having a second bump structure corresponding to the first bump structure;

a planarization layer covering the interlayer insulating layer and the second wiring pattern and including as via-hole that exposes at least a portion of the second wiring pattern; and

a light emission structure contacting the second wiring pattern through the via-hole, and

wherein the first wiring pattern, the interlayer insulating layer, and the second wiring pattern form a capacitor, the light emission structure includes an organic light emitting diode, and the capacitor is directly connected to an anode of the organic light emitting diode.

20. The organic light emitting display device of claim **19**, wherein the first bump structure includes at least one first protrusion that protrudes in an upward direction, the second bump structure includes at least one second protrusion that protrudes in the upward direction, and cross-sections of the first protrusion and the second protrusion are a part of a circular shape, a part of an elliptical shape, or a part of a polygonal shape.

* * * * *

专利名称(译)	单位像素和包括其的有机发光显示装置		
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[标]申请(专利权)人(译)	三星显示有限公司		
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摘要(译)

单位像素包括电路结构，第一和第二布线图案，层间绝缘层，平坦化层和发光结构。设置在电路结构上的第一布线图案具有第一凸块结构。层间绝缘层覆盖电路结构和第一布线图案。设置在层间绝缘层上的第二布线图案与第一布线图案重叠并具有第二凸块结构。平坦化层覆盖层间绝缘层和第二布线图案，并且包括暴露第二布线图案的至少一部分的通孔。发光结构通过通孔接触第二布线图案。第一布线图案和第二布线图案以及层间绝缘层形成电容器，发光结构包括OLED，并且电容器直接连接到OLED的阳极。

